APPARATUS AND METHOD FOR TRACE STREAM
IDENTIFICATION OF A PROCESSOR RESET

Abstract of the Invention

1 When a RESET signal is generated in a target processor
2 during a test procedure, a reset sync marker is generated
3 in a program counter trace stream. The reset sync marker
4 includes a plurality of packets, the packets identifying
5 that the reset sync marker is the result of a RESET signal.
6 The packets identify the program counter address at the
7 time of the generation of the RESET signal and relate the
8 reset sync marker to a timing trace stream. When the RESET
9 signal is removed, a second (reset-off) sync marker is
10 generated identifying the removal of the RESET signal,
11 identifying the program counter address, and relating the
12 second sync marker to the timing trance stream.
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